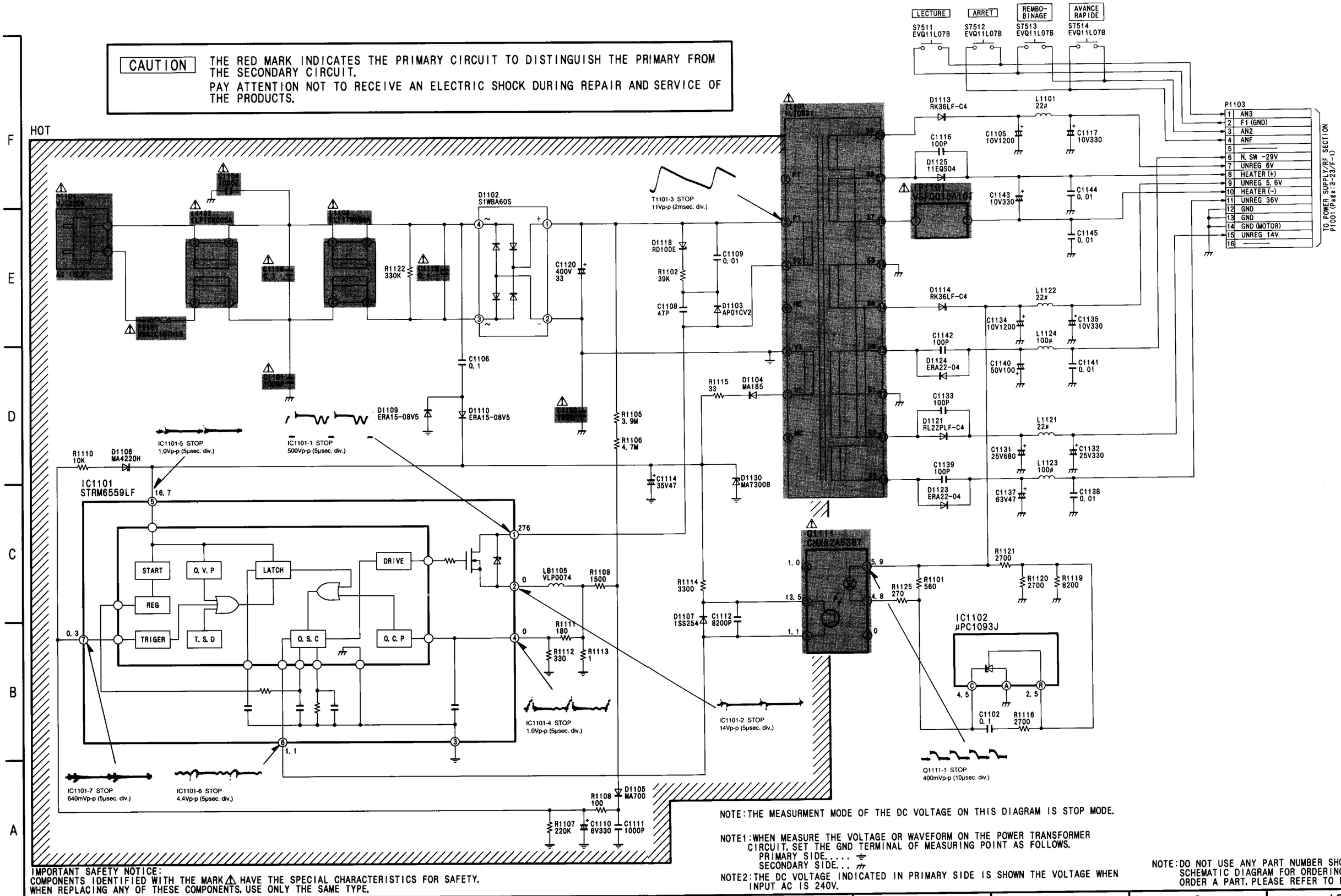
3-6. POWER SCHEMATIC DIAGRAM



NOTE: THE MEASURMENT MODE OF THE DC VOLTAGE ON THIS DIAGRAM IS STOP MODE.

NOTE1: WHEN MEASURE THE VOLTAGE OR WAVEFORM ON THE POWER TRANSFORMER CIRCUIT, SET THE GND TERMINAL OF MEASURING POINT AS FOLLOWS.
PRIMARY SIDE..... ⏚
SECONDARY SIDE... ⏚

NOTE2: THE DC VOLTAGE INDICATED IN PRIMARY SIDE IS SHOWN THE VOLTAGE WHEN INPUT AC IS 240V.

IMPORTANT SAFETY NOTICE:
COMPONENTS IDENTIFIED WITH THE MARK ⚠ HAVE THE SPECIAL CHARACTERISTICS FOR SAFETY.
WHEN REPLACING ANY OF THESE COMPONENTS, USE ONLY THE SAME TYPE.

NOTE: DO NOT USE ANY PART NUMBER SHOWN ON THIS SCHEMATIC DIAGRAM FOR ORDERING. WHEN YOU ORDER A PART, PLEASE REFER TO PARTS LIST.

3-5. Hi-Fi AUDIO BLOCK DIAGRAM

MAIN SIGNAL PATH IN REC MODE

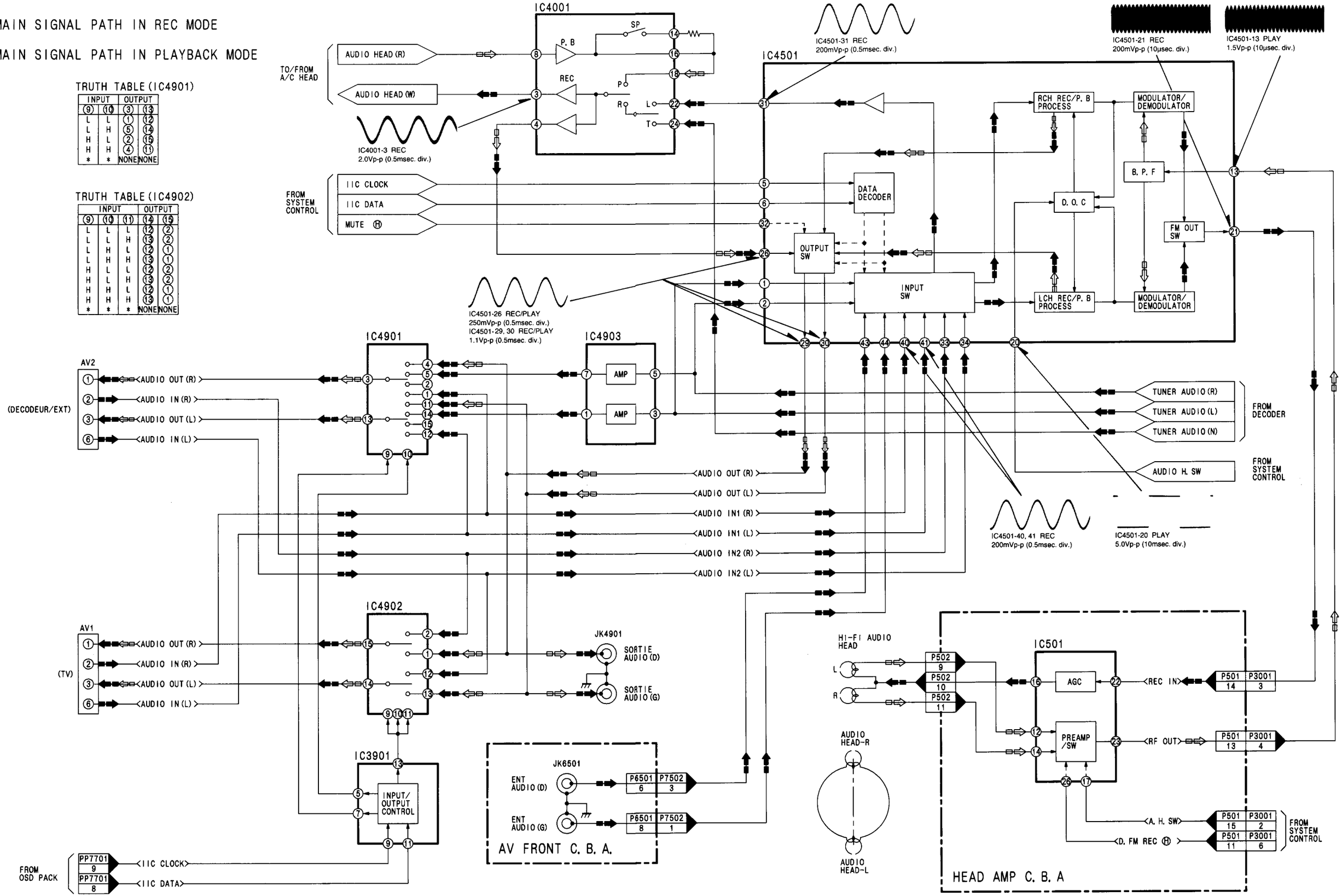
MAIN SIGNAL PATH IN PLAYBACK MODE

TRUTH TABLE (IC4901)

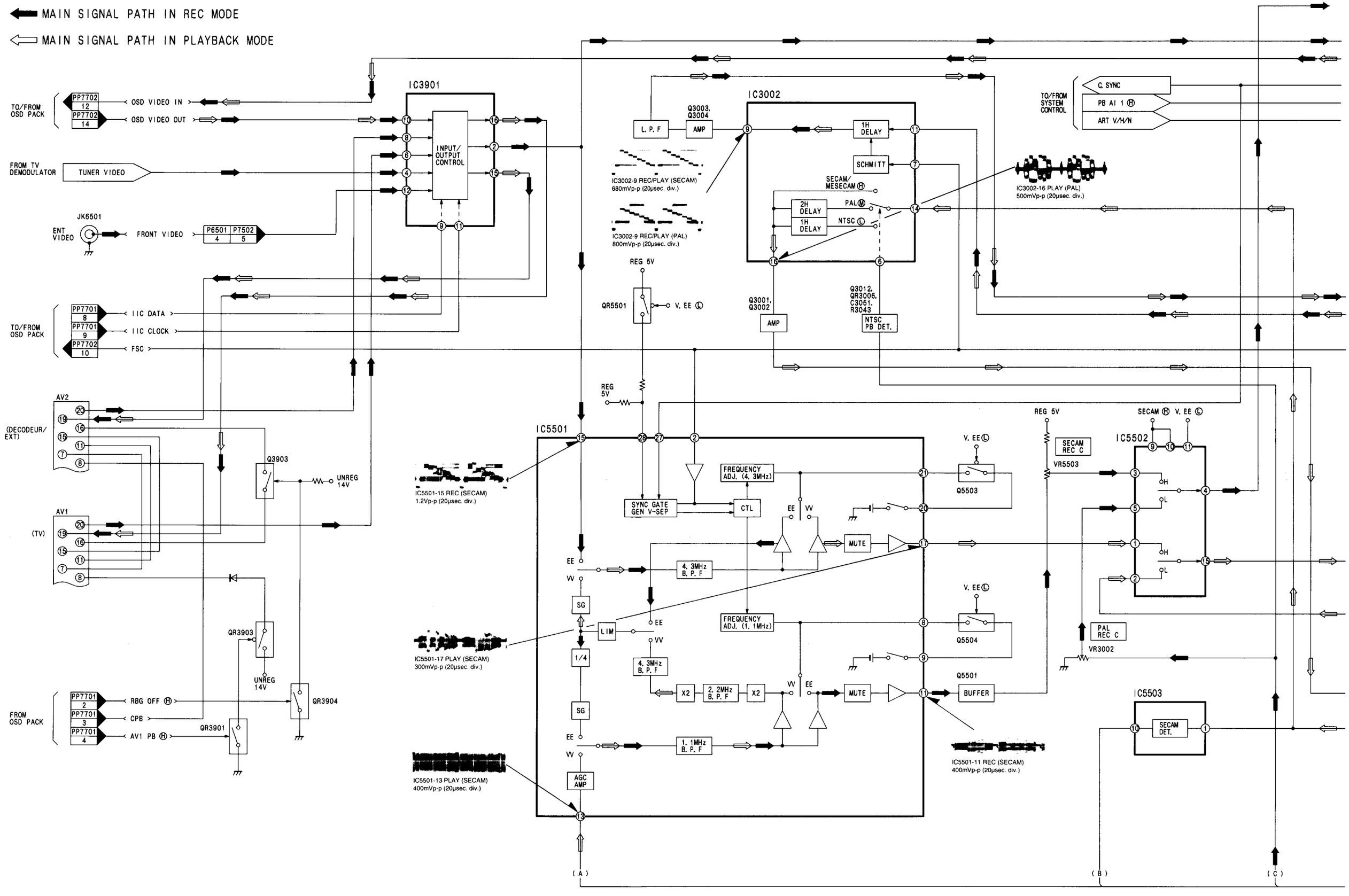
INPUT		OUTPUT	
(9)	(10)	(3)	(13)
L	L	(1)	(12)
L	H	(5)	(14)
H	L	(2)	(15)
H	H	(4)	(11)
*	*	NONE	NONE

TRUTH TABLE (IC4902)

INPUT			OUTPUT	
(9)	(10)	(11)	(14)	(15)
L	L	L	(12)	(2)
L	L	H	(13)	(2)
L	H	L	(12)	(1)
L	H	H	(13)	(1)
H	L	L	(12)	(2)
H	L	H	(13)	(2)
H	H	L	(12)	(1)
H	H	H	(13)	(1)
*	*	*	NONE	NONE



3-4. LUMINANCE & CHROMINANCE BLOCK DIAGRAM



IC3001

AMP
SYNC SEP
MUTE
DETAIL EMPHANSOR
NLE
AGC
CLP
DEV
DET
NLDE
MAIN L. P. F
SUB L. P. F
W/D CLIP
MAIN EMPH
FM MODU
YNR
DOC
H. P. F
Y/C MIX
PIC CONT
NC
LIM
FM DEM
LIM
H. P. F
ENV. DET.
AMP
X2
PHASE SHIFT
+45°
0°
-45°
630KHz B. P. F
MAIN B. P. F
BURST DOWN
ACC
MAIN B. M
BURST UP
630KHz L. P. F
ACC DET.
B. M
B. GENE
BGP
CONV.
THROUGH
PAL
SECAM
KILLER
VCO
ROTARY
APC
VXO
SUB B. M
AFC
X3001
REC/TRICK/PB
SP Ⓛ/PAL-LP Ⓜ /NTSC-LP Ⓗ
MESECAM Ⓗ
B/W Ⓛ
SP Ⓗ
QR3008
V. EE Ⓛ
VV
EE
VV (SP)
VV (LP)

IC3001-41 REC/PLAY (SECAM)
2.0Vp-p (20μsec. div.)
IC3001-43 REC (SECAM)
1.0Vp-p (20μsec. div.)

IC3001-41 REC/PLAY (PAL)
2.2Vp-p (20μsec. div.)
IC3001-43 REC (PAL)
1.1Vp-p (20μsec. div.)

IC3001-39 PLAY (SECAM)
160mVp-p (20μsec. div.)

IC3001-39 PLAY (PAL)
250mVp-p (20μsec. div.)

IC3001-38 PLAY (PAL)
300mVp-p (20μsec. div.)

IC3001-30 PLAY (PAL)
200mVp-p (5msec. div.)

IC3001-28 REC (PAL)
700mVp-p (20μsec. div.)

IC3001-11 REC
1.2Vp-p (20μsec. div.)

IC3001-13 PLAY
800mVp-p (20μsec. div.)

IC3001-19 REC/PLAY
5.0Vp-p (10msec. div.)

Q5502
BUFFER
Q3017, Q3024
BUFFER
TW3030
Q3016
REC Y
VR3003
Q3018
AMP
Q3019
Q3020
QR3005
SECAM Ⓗ
Q3011
NTSC PB DET.
Q3005
AMP
Q3021
FREQUENCY COMPENSATOR
Q3022, Q3023
BUFFER
C3092, L3020
627KHz TRAP
LP Q
VR3005
SP Q
VR3004
QR3013
QR3012
LP Ⓗ
SP Ⓗ
QR3010
QR3002
QR5502
QR5503
QR3011
REG 5V
REG 5V
B/W Ⓛ
PP7701
1
FROM OSD PACK

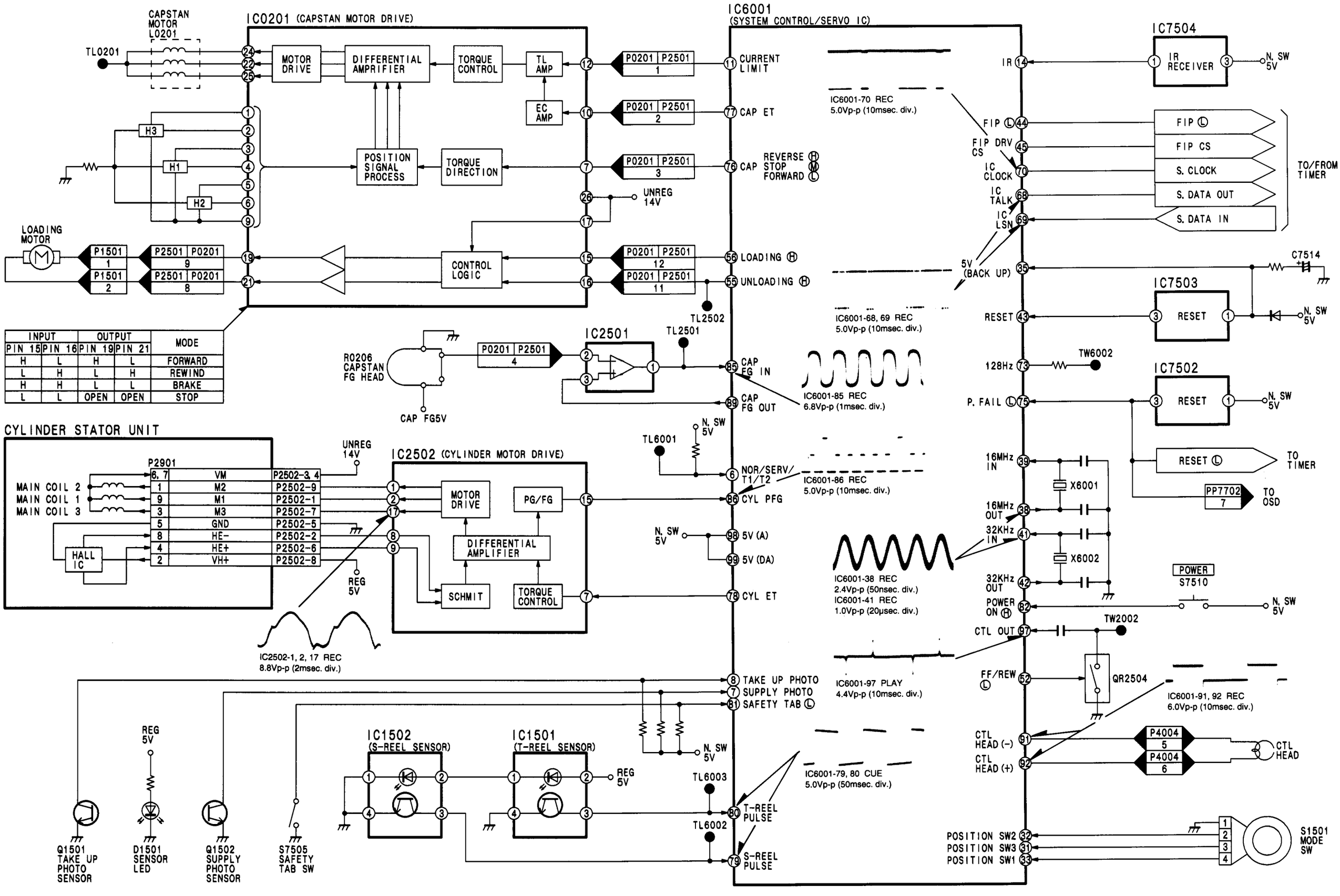
IC501
REC Y+C
AMP & SW
PREAMP & SW
PREAMP & SW
H. AMP SW
RF Y+C
D. REC Ⓗ
LP Ⓗ
HEAD SW
HEAD AMP SW
TRACKING ENV.
ENV. SELECT
TO/FROM SYSTEM CONTROL
TW3001
R (26μm)
L' (49μm)
R' (49μm)
L (26μm)
SP L
SP R
LP L
LP R

P3001 P501
12 5
5 12
11 6
15 2
16 1
7 10
9 8
P502 2
P502 3
P502 4
P502 7
P502 6
P502 5
P501 P3001
4 13

PB AI 2 Ⓗ
PICTURE CTL
ROTARY SW
V. EE Ⓛ
TRICK Ⓛ
SP Ⓛ/LP Ⓗ
NTSC Ⓛ
MESECAM Ⓗ
FROM SYSTEM CONTROL

(A)
(B)
(C)

3-3. SYSTEM CONTROL & SERVO BLOCK DIAGRAM



INPUT		OUTPUT		MODE
PIN 15	PIN 16	PIN 19	PIN 21	
H	L	H	L	FORWARD
L	H	L	H	REWIND
H	H	L	L	BRAKE
L	L	OPEN	OPEN	STOP

3-2. TIMER BLOCK DIAGRAM